31. (Amended) The delay method according to claim 29, wherein, in the delay step, each of the predetermined delay times has a substantially uniform delay time between rising time and falling time of a signal inputted to.

A marked-up copy of the amended claims is attached as required under 37 CFR §1.121.

REMARKS

The above amendments and the following remarks are fully and completely responsive to the Office Action dated January 15, 2002. Claims 1-31 are pending in this application. In the outstanding Office Action, claims 2, 5-9, 18-19, 22-23, 28-29 and 31 were objected to; claims 1-28 were rejected under 35 USC §112, second paragraph; claims 1-4, 6-7, 9-13, 16-18 and 25-31 were rejected under 35 USC §102(b); claims 5, 8, 14-15 and 19-24 were rejected under 35 USC §103(a). No new matter has been entered. Claims 1-31 are presented for consideration.

Claim Objections

Claims 2, 5-9, 18-19, 22-23, 28-29 and 31 were objected to due to the informalities noted in the Office Action. The Applicants thank the Examiner for the suggestions on how to correct these informalities. The amendments to claims 2, 5-9, 18-19, 22-23, 28-29 and 31 correct the informalities in these claims. Accordingly, Applicants respectfully request reconsideration and withdrawal of the objections to claims 2, 5-9, 18-19, 22-23, 28-29 and 31.

35 USC §112, second paragraph

Claims 1-28 were rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctively claim the subject matter which Applicants regard as the invention. Claims 1-3, 18-19, 21, 25-26, and 28 as amended, particularly point out and distinctively claim the subject matter which Applicants regard as the invention. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-28 under 35 USC §112, second paragraph.

35 USC §102(b)

Claims 1-4, 6-7, 9-13, 16-18 and 25-31 were rejected under 35 USC §102(b) as being anticipated by Marbot (U.S. Patent No. 5,521,540). In making this rejection, the Office Action asserts that this reference teaches each and every element of the claimed invention.

Claim 1 recites a delayed circuit. This circuit includes a delayed section having two or more predetermined delayed stages. Each predetermined delayed stage adds a predetermined delay time to an input signal. A selecting switch section establishes a delay path for the input signal by selecting one of the selecting switch sections. At least one of the selecting switch sections include a buffer section for receiving delayed input signal for one of the delayed stages and a selecting section directly connected to the buffer section for activating the buffer section to establish the delay path. Thus, the output signal from the delay path has a desired delay time.

Marbot discloses a delay circuit that includes a plurality of modules U0-U4. Each module is controlled by a respective selection signal a0-a4 and includes a charging circuit

PC and a discharging circuit DC, which are controlled by the associated signal. The charging circuit PC includes a variable resistor R0* and two switches P0 and SW0*. The discharging circuit is formed by a variable resistor R0 and two switches N0 and SW0. The switches SW0 and SW0* are controlled by the selection signal a0 associated with the module U0. The variable resistors of the even-numbered modules are controlled in such a way as to assume a value that is inversely proportional to the coefficient K. The odd-numbered variable resistors are controlled in such way to assume a value inversely proportional to 1-K. When the first two modules U0 and U1 are selected, the variable resistors and the structural capacitance of the line L will define the RC time constant of the charging circuit PC and the discharging circuit DC. The coefficient K is also used to determine the voltage value to which line L will discharge to when switch N0 closes and switch P0 opens.

One object of the present invention is to accurately generate delay signals having a predetermined delay time and delay pulses having predetermined time width. These delay signals are generated by adding delay time to propagating signals derived from input signals without delay and deformation of waveform caused by parasitic elements. In particular, the present invention lets short pulses, capable of coping with high-speed operation, delay accurately without destroying the pulse waveform. In contrast, the object of Marbot is to realize "linear adjustment" with respect to delay signals.

In the present invention, a buffer section and a selecting section are directly connected to each other to reduce parasitic delays caused by resistance elements, capacitance elements or the like. Accordingly, there is no appreciable delay between the buffer section and the selecting section. In Marbot, the "variable resistor" between the

"first and second switch means (P0, N0, SW0,...P4, N4, SW4)" provides "linear adjustment" in the RC time constant. The "variable resistor" has a resistance value inversely proportional to K or 1-K. K is a value between zero and one, thus, a resistance value of zero cannot be obtained. Therefore, Marbot fails to teach the direct connection recited in the present claims. Accordingly, structure of the present invention cannot be anticipated by Marbot.

In the present invention, the delay section generates delay signals. The selecting switch sections each of which includes a buffer section and a selecting section select a predetermined delay signal generated at the delay section by selectively switching the selecting section. Accordingly, only one of the selecting switch sections is selected so as to obtain desired delay signal. Consequently, this structure prevents unnecessary current from flowing between adjoining selecting switch sections, whereby low power consumption can be realized during high-speed operation. In contrast, the desired delay signal, in Marbot, is obtained by adjusting the delay time with the CR time constant of two adjacent modules. Adjusting the delay time requires adjoining modules to concurrently conduct. However, when adjoining modules conduct concurrently, current flows from the power source to ground. Consequently, low power consumption cannot be realized with Marbot's structure.

In the present invention, the buffer section and selecting section are directly connected, and parasitic delays reduced and/or eliminated. Consequently, signals propagate in the shortest length of signal transition time. Accordingly, propagation delays of signals and deformation of signal waveforms are eliminated. Therefore, pulses having a desirable predetermined delay time can be accurately output. In contrast, Marbot, adjusts

the delay time by adjusting the CR time constant in accordance with a resistance value provided for a current path formed between adjoining modules when the both of the adjoining modules concurrently conduct. In order to adjust delay time, the signal transition period between adjoining modules for each of the adjoining modules must coincide with each other. Accordingly, signal transition time at each module becomes long and short pulses cannot be propagated accurately. Therefore, Marbot teaches a variable resistor between the "buffer" and "selecting" section in order to adjust the delay time. In contrast, the present claims recite a direct connection between the "buffer" and "selecting" sections. Consequently, Marbot fails to teach the claimed invention. Accordingly, Applicants request reconsideration and withdrawal of the rejection under 35 USC §102(b).

35 USC §103(a)

Claims 5, 8, 14-15, and 19-24 were rejected under 35 USC §103(a) as being unpatentable over Marbot. In making this rejection, the Office Action asserts that these claims are either obvious in view of Marbot, or suggested by Marbot. Applicants request reconsideration.

As discussed in detail above, Marbot fails to teach and/or suggest a direct connection between the buffer section and the selection section. Therefore, Marbot fails to teach and/or suggest the claimed invention. Accordingly, Applicants request reconsideration and withdrawal of the rejection under 35 USC §103(a).

Conclusion

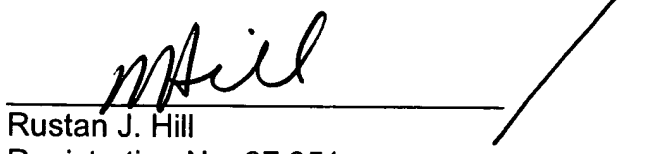
Applicants' amendments and remarks have clearly overcome the objection and rejections set forth in the Office Action dated January 15, 2002. Specifically, the

amendments to claims 2, 5-9, 18-19, 22-23, 28-29 and 31 overcome the objection to these claims. The amendment to claims 1-2, 3, 18-19, 21, 25-26 and 28 overcome the rejection to claims 1-28 under 35 USC §112, second paragraph. Applicants' remarks have clearly overcome the rejection of claims 1-4, 6-7, 9-13, 16-18 and 25-31 under 35 USC §102(b). Applicants' remarks have also distinguished claims 5, 8, 14-15 and 19-24 under 35 USC §103(a). Accordingly, claims 1-31 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-31.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned Attorney by telephone, if it is believed that such contact will expedite the prosecution of the application.

The Commissioner is authorized to charge payment for any additional fees, which may be required with respect to this paper, to Deposit Account No. 01-2300 making reference to Attorney Docket No. 024016-00012.

Respectfully submitted,



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MARKED-UP COPY OF AMENDED CLAIMS AS REQUIRED UNDER 37 CFR §1.121

1. (Amended) A delay circuit comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a [in which] predetermined delay time [is added] to an input signal; and

selecting switch sections for [combining the predetermined delay stages as appropriate and] establishing a delay path for the input signal by selecting one of the selecting switch sections [that outputs a delayed output signal having the desired delay time], wherein

at least one of the selecting switch sections comprise:

a buffer section [sections for inputting propagated] for receiving delayed input signal [signals] from one of the delay stages [the input signal]; and

a selecting section directly connected to the buffer section [sections] for activating the buffer section [sections when] to establish the delay path [is being established in the delay section], and wherein

an output signal from the delay path has a desired delay time.

2. (Amended) The delay circuit according to claim 1, wherein[, in the delay section, the] at least one of the predetermined delay stages [are] is provided with an individual delayed output [terminals] terminal for outputting an individual delayed output [signals] signal having [the] an individual predetermined delay time [times], and wherein at least one selecting switch [sections are] section is provided for each individual

delayed output [terminals] terminal with an input [terminals] terminal of the buffer [sections] section [in the selecting switch sections] being connected to the individual delayed output [terminals] terminal and output terminals of the selecting switch sections being mutually joined.

3. (Amended) The delay circuit according to claim 1, wherein[, in the delay section, the] at least one predetermined delay [stages are] stage is provided with an individual delay input [terminals] terminal for inputting [signals] a signal to which the predetermined delay time is [times are to be] added, [and] the rise delay time and fall delay time for the [input signals] signal inputted to each of the predetermined delay stages are [balanced so as to be] substantially uniform, and wherein at least one selecting switch [sections are] section is provided for each individual delay input [terminals] terminal with [output] an output terminal [terminals] of the selecting switch [sections] section being connected to the individual delay input terminal [terminals] and input terminals of the buffer sections being mutually joined.

4. (Amended) The delay circuit according to claim 1, wherein, [in the selecting switch sections,] the buffer section is [sections are] provided with a first transistor [transistors] whose gate [terminals are] terminal is set as an input terminal [terminals], and the selecting [sections are] section is provided with a second [transistors] transistor into whose gate [terminals] terminal a control [signals] signal for establishing the delay path in the delay section [are] is input, and the first and second

transistors are connected directly in series between the output [terminals] terminal of the selecting switch [sections] section and a first power supply voltage.

5. (Amended) The delay circuit according to claim 4, wherein the first [transistors are] transistor is [provided at] connected between the second transistor and the output terminal [side of the selecting switch sections and the second transistors are provided at the first power supply voltage side].

6. (Amended) The delay circuit according to claim 4, wherein the first [transistors are] transistor is [provided at] connected between the second transistor and the first power supply voltage [side and the second transistors are provided at an output terminal side of the selecting switch sections].

7. (Amended) The delay circuit according to claim 4, wherein[, in the selecting switch sections,] the buffer [sections are] section further [provided with] comprises a third [transistors] transistor whose gate [terminals are set as] terminal is connected to the input [terminals] terminal, and the selecting [sections are] section further [provided with] comprises a fourth [transistors] transistor into whose gate [terminals] terminal the control [signals] signal for establishing the delay path in the delay section [are] is input, and the third and fourth transistors are connected directly in series between the output [terminals] terminal of the selecting switch [sections] section and a second power supply voltage.

8. (Amended) The delay circuit according to claim 7, wherein the first [and third transistors are provided at an] transistor is connected between the second transistor and the output terminal [side] of the selecting switch [sections the second transistors are provided at the first power supply voltage side, and the fourth transistors are provided at the second power supply side,] section and the third transistor is connected between the fourth transistor and the output terminal.

9. (Amended) The delay circuit according to claim 7, wherein the second [and fourth transistors are provided at an] transistor is connected between the first transistor and the output terminal [side] of the selecting switch [sections the first transistors are provided at the first power supply voltage side, and the third transistors are provided at the second power supply side,] section and the fourth transistor is connected between the third transistor and the output terminal.

14. (Amended) The delay circuit according to claim 4, wherein drive capacity of the second [transistors are] transistor is larger than drive capacity of the first [transistors] transistor.

15. (Amended) The delay circuit according to claim [4] 7, wherein drive capacity of the fourth [transistors are] transistor is larger than drive capacity of the third [transistors] transistor.

16. (Amended) The delay circuit according to claim 2, wherein, in the delay section, the individual delayed output [terminals are] terminal is connected to an input [terminals] terminal of the next one of the predetermined delay [stage] stages and a plurality of the predetermined delay stages are connected in series.

17. (Amended) The delay circuit according to claim 3, wherein, in the delay section, the output [terminals] terminal of each of the predetermined delay stages [are] is connected to [the next] the individual delayed input [terminals] terminal of the next one of the predetermined delay stages and a plurality of the predetermined delay stages are connected in series.

18. (Amended) The delay circuit according to claim 16, wherein, in [the] at least one of the predetermined delay stages, the rise delay time and fall delay time for [an input] a signal inputted to each of the predetermined delay stages are [balanced so as to be] substantially uniform.

19. (Amended) The delay circuit according to claim 18, wherein each of the predetermined delay [stages are formed with a basic unit being a unit delay stage in which] stages comprise an even number of logic inversion sections connected in series, in which the rise delay time and fall delay time for [an] the [input] signal are [balanced so as to be] substantially uniform[, are connected in series].

21. (Amended) The delay circuit according to claim [18] 16, wherein each of the predetermined delay [stages are formed with a basic unit being a unit delay stage in which an] stage comprises an even number of logic inversion sections connected in series, in which the rise delay time and fall delay time of [an input] the signal are different[, are connected in series].

22. (Amended) The delay circuit according to claim 21, wherein each of the logic inversion sections [are] is a NAND [gates] gate that [form] forms inverted logic through input terminals other than the input [terminals] terminal into which the [propagated signals are] signal is input being connected to [the] a power supply voltage potential.

23. (Amended) The delay circuit according to claim 21, wherein each of the logic inversion sections [are] is a NOR [gates] gate that [form] forms inverted logic through input terminals other than the input [terminals] terminal into which the [propagated signals are] signal is input being connected to [the] a ground potential.

25. (Amended) The delay circuit according to claim 4, wherein, when the delay path in the delay section is established using [a logic combination of] two or more [composite] control signals, there is provided instead of the second transistor, [or fourth transistors, transistor series having the same functions as the second or fourth transistors and formed from] two or more transistors connected in series into whose respective gate terminals the respective [composite] control signals are input.

26. (Amended) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages, [in which] each predetermined delay stage adds a predetermined delay time [is added] to an input signal; and

selecting switch sections for establishing a delay path for the input signal by selecting one of the selecting switch sections, wherein at least one of the selecting switch sections comprise:

a buffer [sections] section for [inputting propagated signals] receiving delayed input signal from [the input signal] one of the delay stages ; and

a selecting [sections] section directly connected to the buffer section for activating the buffer section to establish the delay path, and wherein [for establishing a delay path in the delay section;

wherein the selecting switch sections combine the predetermined delay stages as appropriate and establish a delay path for the input signal that outputs a delayed] an output signal from the delay path [having the] has a desired delay time.

27. (Amended) The semiconductor integrated circuit device according to claim 26, wherein, [in the selecting switch sections,] the buffer [sections] section [are] is provided with a first [transistors] transistor whose gate [terminals are] terminal is set as an input [terminals] terminal, and the selecting [sections] section [are] is provided with a second [transistors] transistor into whose gate [terminals] a terminal control [signals] signal for establishing the delay path in the delay section [are] is input, and the first and

second transistors are connected directly in series between the output terminal [terminals] of the selecting switch [sections] section and a first power supply voltage.

28. (Amended) The semiconductor integrated circuit device according to claim 26, wherein, in at least one of the predetermined delay stages, the rise delay time and fall delay time for [an input] a signal inputted to each of the predetermined delay stages are [balanced so as to be] substantially uniform.

29. (Amended) A delay method comprising:

a delay step in which predetermined delay times are sequentially added onto an input signal to obtain delay signals;

[an output step in which delay signals are output for each predetermined delay time added in the delay step; and]

a selecting step which is [only] activated only when [a] one of the delay [signal] signals [having the desired delay time is output] in the [output] delay step has a desired delay time; and

an output step in which one of the delay signals in the delay step is output by activating the selecting step.

31. (Amended) The delay method according to claim 29, wherein, in the delay step, each of the predetermined delay times [have] has a substantially uniform delay time [formed by the rise delay] between rising time and [the fall delay] falling time of [the input] a signal inputted to.